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**CLASS : S.E. COMP SUBJECT : DEL**

**EXPT. NO. : 8 DATE : 11/12/2021**

**TITLE : UP/DOWN COUNTER CIRCUIT**

**OBJECTIVE :**

1. Design and Implement 3-bit Asynchronous (Ripple) UP/DOWN –Counter using Mode control switch (Use-IC-74LS76) and verify its truth-table.

Draw Timing diagram

***When M=0: Circuit perform UP –Counting operation***

***When M=1: Circuit perform DOWN –Counting operation***

1. Design and Implement 2-bit Asynchronous UP/DOWN –Counter using Mode control switch (Use-IC-74LS76) and verify its truth-table.

Draw Timing diagram

***When M=0: Circuit performs UP –Counting operation***

***When M=1: Circuit performs DOWN –Counting operation***

**APPARATUS :**

Digital-Board, GP-4 Patch-Cords, IC-74LS76, IC-74LS90, IC-74LS191, IC-74LS32, IC74LS04/IC-74LS08 and Required Logic gates if any

**THEORY :**

Counter is a Sequential Logic device which can be use to count the number of pulses given to the circuit. Counter can be classified into two category one is Synchronous and other is Asynchronous (Ripple) In case of Asynchronous counter output of first flip-flop goes to the clock of next and so on, and input of all flipflop is connected to VCC for IC-74LS76.

All set and reset pin is connected to VCC. Asynchronous counter is easy to design as compared to Synchronous Counter. Synchronous Counter is faster than Asynchronous Counter.IC-74LS76 is Dual M/S-JK filp-flop, which means in one IC there are two M/S-JK filp-flop are contained.

IC -7490 is called as a 4-bit MS-JK Flip-flop decade (BCD) Ripple counter. It contains 4 -master slave flip flops internally connected to provide MOD-2 i.e. divide by 2 and MOD-5 i.e. divide by 5 counter.MOD-2 and Mod-5 counters can be used independently or in cascading. Each Counter has a separate clock input to initiate state changes of the counter on the high to low clock transition. Since the o/p from the divide by 2 section is not internally connected to the succeeding stages. The device may be operated in various counting modes. In a BCD counter the CP1 input must be externally connected to Q0 output. The CP0 input receives the incoming count producing a BCD count sequence.

It is also provided with additional gating to provide a divide by 2 counter and binary counter for which the count cycle length is divide by 5. The device may be operated in various counting modes.

There are 2 reset inputs R0 (1) and R0 (2) both of which need to be connected to the ‘logic 1’ for clearing all flip flops. Two set inputs Rg(1) and Rg(2) when connected to logic are used for setting counter to 1001 (BCD 9).IC74191 is 4-bit binary parallel presettable Programmable UP/DOWN synchronous counter. It contains 4 master slave J-K flip flops with internal gating and steering logic to provide asynchronous reset and synchronous count up/down operations; its asynchronous parallel capability permits the counter to be preset to any desire number. D0 to D3 are the parallel data inputs. Information present on the parallel data inputs D0 to D3 is loaded into the counter and appears on the output when the load **PL** input is lowthisoperation is overrides the counting function .counting is inhabited by the high level on the enable CE input, when CE input is low internal state changes are initiated synchronously by the low to high transitions of the clock inputs the up/down input signal determines the direction of input.

**PIN Diagram :**

PRESET1

PRESET2

CLOCK1

CLEAR1

CLEAR2

1

K

J

2

1

Q

1

Q

GND

K

2

Q

2

Q

2

CLOCK2

J

1

VCC

7

4

LS

7

6

D

U

A

L

MS

J-K

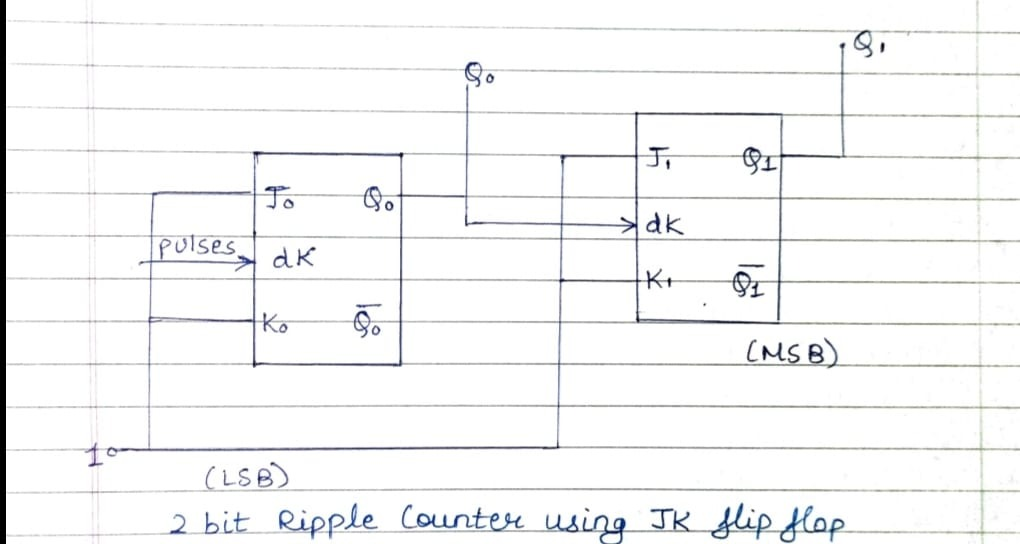
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**PROCEDURE :**

1. Make the connections as per the Logic circuit of 3-bit Asynchronous UP/ DOWN Counter circuit using IC-74LS76 and Verify its Truth Table.
2. Make the connections as per the Logic circuit of 2-bit Synchronous UP/ DOWN Counter circuit using IC-74LS76 and Verify its Truth Table.

# Design of 2-bit (Ripple) UP/DOWN-Counter Using Mode control S/W

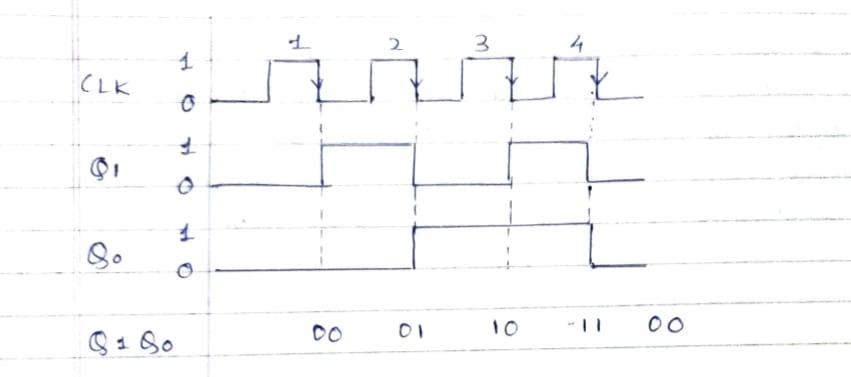
**Logic diagram:**



**Observation Table:**

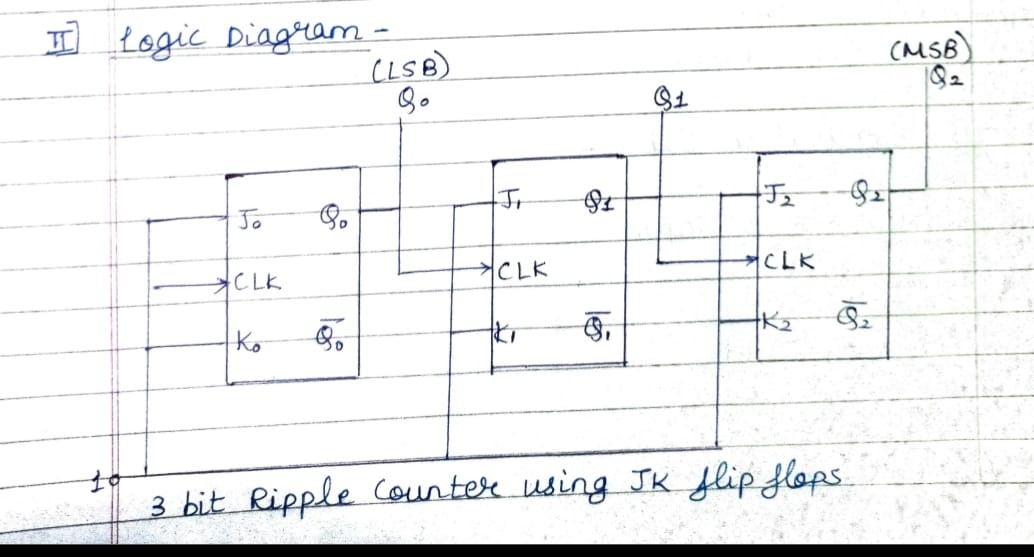
|  |  |  |
| --- | --- | --- |
| **Number of input pulses** | **Output** | |
| **Q1** | **Q0** |
| **0** | **-** | **-** |
| **1** | **0** | **0** |
| **2** | **0** | **1** |
| **3** | **1** | **0** |
| **4** | **1** | **1** |

**Timing Diagram:**



# Design of 3-bit (Ripple) UP/DOWN-Counter Using Mode control S/W

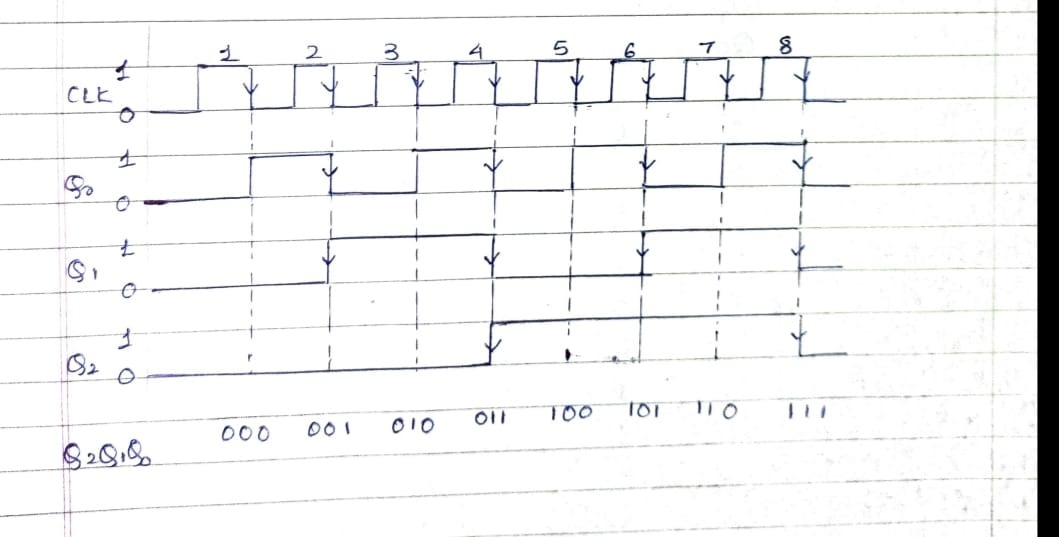
**Logic diagram:**



**Observation Table:**

|  |  |  |  |
| --- | --- | --- | --- |
| **Number of Pulses** |  | **Output** |  |
| **Q2** | **Q1** | **Q0** |
| **0** | - | **-** | **-** |
| **1** | **0** | **0** | **0** |
| **2** | **0** | **0** | **1** |
| **3** | **0** | **1** | **0** |
| **4** | **0** | **1** | **1** |
| **5** | **1** | **0** | **0** |
| **6** | **1** | **0** | **1** |
| **7** | **1** | **1** | **0** |
| **8** | **1** | **1** | **1** |

**Timing Diagram:**



**Logic Gates / MSI Device required for Implementation:**

|  |  |  |
| --- | --- | --- |
| **Sr.No.** | **Title** | **Name of the IC** |
| 01 | 3-bit Ripple UP/DOWN Counter | 74LS76 |
| 02 | 2-bit Asynchronous UP/DOWN Counter | 74LS76 |

**CONCLUSION:**

From this experiment, we have learnt to implement 2-bit and 3-bit asynchronous/ripple UP/DOWN counter using IC 74LS76.

**REFFRENCE:**

1. **R.P.Jain “Modern Digital Electronics” TMH 4th Edition**

1. **D.Leach,Malvino,Saha,”Digital Principles and Applications”,TMH**

Subject teacher Sign with Date Remark